Amendments to the Claims:

Please replace all prior versions, and listings of claims in the application with the following listing of claims.

Listing of claims

Claim 1 (currently amended): A data processing architecture comprising:

an input device for receiving an incoming stream of data packets; and

a plurality of processing elements which are operable to process data received thereby;

wherein ~~for any given data processing bandwidth of the processing elements~~ the input device is operable to distribute whole data packets of potentially varying size across one or more processing elements such that the number of processing elements across which each whole data packet is distributed is dynamically determined based at least in part on the size of the whole data packet.

Claim 2 (original): A data processing architecture as claimed in claim 1, wherein the processing elements are arranged in a single instruction multiple data (SIMD) array.

Claim 3 (previously presented): A data processing architecture as claimed in claim 1, wherein a whole data packet is allocated to as many processing elements as are necessary to store it and to process it.

Claim 4 (original): A data processing architecture as claimed in claim 1, wherein the input device is operable to divide the incoming data packet stream into processor data packets of a fixed size for distribution to the processing elements.

Claim 5 (previously presented): A data processing architecture as claimed in claim 4, wherein the input device is operable to distribute a whole packet or a said processor data packet part to a processing element.

Claim 6 (original): A data processing architecture as claimed in claim 1, wherein the input device is operable to transfer data packets to the processing elements such that not all processing elements receive data.

Claim 7 (original): A data processing architecture as claimed in claim 1, wherein the processing elements are operable to control the input device.

Claim 8 (original): A data processing architecture as claimed in claim 7, wherein the processing elements are operable to control the input device by means of software.

Claim 9 (original): A data processing architecture as claimed in claim 1, wherein the processing elements are operable to control an output device.

Claim 10 (canceled)

Claim 11 (previously presented): A data processing architecture as claimed in claim 60, comprising a plurality of such input/output systems, adapted to support multiple input/output operations.

Claim 12 (currently amended): A data processing architecture as claimed in claim 1, comprising a single instruction multiple data (SIMD) data processing ~~architecture~~ architecture,

wherein at least one processing element is operable to enter a standby mode of operation in dependence upon data received by that processing element.

Claim 13 (previously presented): A data processing architecture as claimed in claim 12, wherein the at least one processing element is operable to enter the standby mode of operation when no data is received.

Claim 14 (original): A data processing architecture comprising:

a parallel array of processing elements arranged in a single instruction multiple data processing array;

a hardware accelerator unit operable to receive, in series, processing requests from the processing elements and to return processing results to respective processing elements when those processing results are available; and

an input/output system which is operable to transfer respective processing requests from the processing elements to the hardware accelerator, and to return processing results to the processing elements concerned,

wherein the processing elements are operable to process the returned processing results when all such results are returned, or after a predetermined time period.

Claim 15 (original): A data processing architecture comprising:

a parallel array of processing elements arranged in a single instruction multiple data processing array;

a hardware accelerator unit operable to receive, in series, processing requests from the processing elements and to return processing results to respective processing elements in the order in which processing requests were received by the accelerator unit; and

an input/output system which is operable to transfer respective processing requests from the processing elements to the hardware accelerator, and to return processing results to the processing elements concerned,

wherein the processing elements are operable to process the returned processing results when all such results are returned, or after a predetermined time period.

Claim 16 (previously presented): A data processing architecture as claimed in claim 1, comprising a first plurality of parallel arrays of processing elements, and a second plurality of hardware accelerator units.

Claim 17 (previously presented): A data processing architecture as claimed in claim 1, comprising a plurality of parallel arrays of said processing elements, and a data I/O structure which is operable to transfer data to and from the arrays of processing elements in turn.

Claim 18 (canceled)

Claim 19 (previously presented): A data processing architecture as claimed in claim 2, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 20 (original): An architecture as claimed in claim 1, comprising a plurality of functional blocks chosen from: a SIMD processing element array, a data input device, a data output device, a hardware accelerator, a data packet buffer and a bus structure for connecting the functional blocks to one another.

Claim 21 (original): An architecture as claimed in claim 1, implemented on a single integrated circuit.

Claim 22 (original): An architecture as claimed in claim 1, implemented on a plurality of integrated circuits.

Claim 23 (original): An input/output system for transferring data to and from a plurality of processing elements arranged in a single instruction multiple data (SIMD) array, the system being operable to transfer data packets of different sizes to respective ones of the processing elements in the array.

Claim 24 (original): A system as claimed in claim 23, operable to transfer the data packets to respective different addresses in the processing elements.

Claim 25 (original): A system as claimed in claim 23, wherein data packet transfer is controlled by the processing elements in the array.

Claim 26 (original): A system as claimed in claim 23, operable to transfer the data packets to the processing elements when a batch of data packets are ready for transfer in an input device.

Claim 27 (original): A system as claimed in claim 23, operable to transfer the data packets to the processing elements when part of a batch of data packets are ready for transfer in an input device.

Claim 28 (original): A system as claimed in claim 27, wherein the part batch is transferred in response to a request from the processing elements.

Claim 29 (original): A system as claimed in claim 23, operable to transfer data packets from the processing elements to an output device when a full batch has been processed.

Claim 30 (original): A system as claimed in claim 23, operable to transfer data packets from the processing elements to an output device when part of batch has been processed.

Claim 31 (original): A system as claimed in claim 26, wherein the decision to transfer full or part batches is made in dependence upon the speed of the processing elements and the speed and intermittency of the data packets.

Claim 32 (original): A processor comprising an architecture or system as claimed in claim 1.

Claim 33 (original): A data processing architecture as claimed in claim 15, comprising a first plurality of parallel arrays of processing elements, and a second plurality of hardware accelerator units.

Claim 34 (previously presented): An architecture as claimed in claim 60, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 35 (original): An architecture as claimed in claim 12, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 36 (original): An architecture as claimed in claim 14, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 37 (original): An architecture as claimed in claim 15, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 38 (original): An architecture as claimed in claim 17, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 39 (canceled)

Claim 40 (previously presented): An architecture as claimed in claim 60, implemented on a single integrated circuit.

Claim 41 (original): An architecture as claimed in claim 12, implemented on a single integrated circuit.

Claim 42 (original): An architecture as claimed in claim 14, implemented on a single integrated circuit.

Claim 43 (original): An architecture as claimed in claim 15, implemented on a single integrated circuit.

Claim 44 (original): An architecture as claimed in claim 17, implemented on a single integrated circuit.

Claim 45 (canceled)

Claim 46 (previously presented): An architecture as claimed in claim 60, implemented on a plurality of integrated circuit.

Claim 47 (original): An architecture as claimed in claim 12, implemented on a plurality of integrated circuit.

Claim 48 (original): An architecture as claimed in claim 14, implemented on a plurality of integrated circuit.

Claim 49 (original): An architecture as claimed in claim 15, implemented on a plurality of integrated circuit.

Claim 50 (original): An architecture as claimed in claim 17, implemented on a plurality of integrated circuit.

Claim 51 (canceled)

Claim 52 (previously presented): A processor comprising an architecture or system as claimed in claim 60.

Claim 53 (original): A processor comprising an architecture or system as claimed in claim 12.

Claim 54 (original): A processor comprising an architecture or system as claimed in claim 14.

Claim 55 (original): A processor comprising an architecture or system as claimed in claim 15.

Claim 56 (original): A processor comprising an architecture or system as claimed in claim 17.

Claim 57 (canceled)

Claim 58 (original): A processor comprising an architecture or system as claimed in claim 23.

Claim 59 (previously presented): A data processing architecture as claimed in claim 9, wherein said output device is operable to collect processor data packets from the processing elements and to construct an outgoing data packet stream from collected processor data packets.

Claim 60 (previously presented): A data processing architecture as claimed in claim 9, wherein said input device and said output device are part of an input output system operable to transmit data to, and receive data from, the processing elements.